

What is Claimed is:

1. A programmable logic device comprising:
digital signal processing circuitry
comprising at least one embedded multiplier of a
particular size; and
5 programmable logic circuitry, wherein a
user logic design multiplier of a size greater than the
particular size is implemented by a user logic design
to hardware application using the at least one embedded
multiplier and the programmable logic circuitry.
2. The programmable logic device of claim 1
wherein:
the programmable logic circuitry is
configured to implement at least one component
5 multiplier; and
the at least one component multiplier
and the at least one embedded multiplier generate
partial products, the sum of which is the product of
the user logic design multiplier.
3. The programmable logic device of claim 2
wherein the additional component multiplier is a single
embedded multiplier selected from the at least one
embedded multiplier.
4. The programmable logic device of claim 2
wherein the at least one component multiplier comprises
three component multipliers implemented using
programmable logic circuitry.
5. The programmable logic device of claim 2
wherein the at least one component multiplier comprises

two component multipliers implemented using programmable logic circuitry.

6. The programmable logic device of claim 2 wherein:

the user logic design multiplier has a size that exceeds the particular size of the at least one embedded multiplier by one bit on one side of the at least one embedded multiplier; and

the at least one component multiplier comprises a single component multiplier implemented using programmable logic circuitry.

7. The programmable logic device of claim 2 further comprising circuitry for generating the sum of partial products of the at least one component multiplier and the at least one embedded multiplier.

8. The programmable logic device of claim 1 wherein the particular size a largest size available among all embedded multipliers in the programmable logic device that is still smaller than the size of the user logic design multiplier.

9. A method for implementing a user logic design multiplier of a particular size in a programmable logic device having one or more embedded multipliers implemented in digital signal processing circuitry using a user logic design to hardware application, the method comprising:

selecting one of the embedded multipliers having a size that is less than the particular size; and

configuring programmable logic circuitry in the programmable logic device to implement a sum of

partial products, including in the sum, a product
generated by the selected embedded multiplier, the sum
of partial products being the product of the user logic
15 design multiplier.

10. The method of claim 9 wherein the
configuring programmable logic circuitry comprises
determining partial products to use with the product
generated by the selected embedded multiplier to
5 implement the sum of partial products.

11. The method of claim 10 wherein the
determining partial products to use comprises
determining a number of partial products to use with
the product generated by the selected embedded
5 multiplier to implement the sum of partial products.

12. The method of claim 11 wherein the
determining a number of partial products to use
comprises determining to use two partial products with
the product generated by the selected embedded
5 multiplier to implement the sum of partial products.

13. The method of claim 11 wherein the
determining a number of partial products to use
comprises determining to use three partial products
with the product generated by the selected embedded
5 multiplier to implement the sum of partial products.

14. The method of claim 9 further comprising
determining a circuit implementation for generating the
sum of partial products.

15. The method of claim 9 wherein the
selecting one of the embedded multipliers having a size

that is less than the particular size comprises
selecting one of the embedded multipliers having a size
5 that is a largest size available among the embedded
multipliers that is still smaller than the particular
size.

16. The method of claim 15 further
comprising:

determining that the one of the embedded
multipliers has a size that is exceeded by the
5 particular size by one bit on one side of the user
logic design multiplier; and

determining to use one partial product
with the product generated by the selected embedded
multiplier to implement the sum of partial products.

17. Machine-readable media encoded with
machine-readable instructions for implementing a user
logic design multiplier of a particular size in a
programmable logic device having one or more embedded
5 multipliers implemented in digital signal processing
circuitry using a user logic design to hardware
application, the machine-readable instructions encoded
for perform the method of:

selecting one of the embedded
10 multipliers having a size that is less than the
particular size; and

configuring programmable logic circuitry
in the programmable logic device to implement a sum of
partial products including in the sum a product
15 generated by the selected embedded multiplier, the sum
of partial products being the product of the user logic
design multiplier.

18. A printed circuit board on which is mounted a programmable logic device as defined in claim 1.

19. The printed circuit board defined in claim 18 further comprising:

a memory mounted on the printed circuit board and coupled to the memory circuitry.

20. The printed circuit board defined in claim 18 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

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